REMARKS

In response to the Office Action dated June 7, 2006, Applicants respectfully request reconsideration based on the above amendments and the following remarks. Applicants respectfully submit that the claims as presented are in condition for allowance.

Claims 1 and 8 were objected to. Claim 1 has been amended to address the item raised by the Examiner. Claim 8 has been amended to clarify the difference between the first and second operational modes. In the first operational mode, different techniques are used depending on whether a cache hit or cache miss is present. In the second operational mode, the cache hit/miss does not alter the functionality. Thus, Applicants assert that the first and second operational modes are claimed as being different operations.

Claims 1-3 and 8-10 were rejected under 35 U.S.C. § 103 as being unpatentable over Ishimi in view of Baron. This rejection is traversed for the following reasons.

Claim 1 recites, *inter alia,* "said placing said cache in the second operational mode including setting a memory mode bit, the memory mode bit logically combined with a write command pulse to generate a memory mode write pulse; writing said data to said cache regardless of whether a write miss is present or absent to update a cache directory with the contents of a target address, said writing said data including a logical operation of the memory mode write pulse and a cache hit write pulse, wherein in the absence of a cache hit write pulse, said data is written to said cache in the presence of said memory mode write pulse." As shown in Figure 2, for example, when the memory mode bit is active and a write command pulse is present, the memory mode write pulse (memory_mode_wrt_1PULSE) is active. This pulse is then logically operated on and logically combined (e.g., ORed) with results from an ANDing operations such that if the memory mode write pulse is present, there is no need for a cache hit write to be present.

Ishimi fails to teach the operation recited in claim 1. As shown in Figure 4 of Ishimi, a memory mode bit 9 is not logically combined with the cache hit signal 11. Thus, Ishimi fails to teach the processing recited in claim 1.

Baron was relied upon for allegedly disclosing interaction between the memory mode bit, the write command pulse, the memory mode write pulse and the cache hit write pulse. Baron fails to teach the claimed interaction of these elements. In interpreting Baron, the

Examiner submits that the CE bit is logically combined with the PAB to write to memory 10. Baron, however, fails to teach the "the memory mode bit logically combined with a write command pulse to generate a memory mode write pulse" and then "a logical operation of the memory mode write pulse and a cache hit write pulse." In claim 1, the memory mode bit and the write command pulse generate a memory mode write pulse. This memory mode write pulse is then combined with the cache hit write pulse. This processing is not taught in Baron. At best, Baron combines the CE with the PAB address, but there is no teaching of the bit and three pulses recited in claim 1. Even if Ishimi and Baron are combined, the features of claim 1 do not result.

For the above reasons claim 1 is patentable over Ishimi and Baron. Claims 2-3 depend from claim 1 and are patentable over Ishimi and Baron for at least the reasons advanced with reference to claim 1. Claim 8 recites features similar to those discussed above with reference to claim 1 and is patentable over Ishimi and Baron for at least the reasons advanced with reference to claim 1. Claims 9-10 depend from claim 8 and are patentable over Ishimi and Baron for at least the reasons advanced with reference to claim 1.

Claims 4, 5, 11 and 12 were rejected under 35 U.S.C. § 103 as being unpatentable over Ishimi in view of Baron and Dosaka. Dosaka was relied upon for allegedly designating an operational mode based on address bits. Dosaka does not cure the deficiencies of Ishimi and Baron discussed above with reference to claims 1 and 8, upon which claims 4, 5, 11 and 12 depend. Thus, claims 4, 5, 11 and 12 are patentable over Ishimi in view of Dosaka for at least the reasons advanced with reference to claim 1.

Claims 7 and 14 were rejected under 35 U.S.C. § 103 as being unpatentable over Ishimi in view of Baron and Anthony. Anthony was relied upon for allegedly disclosing a select all bins bit to invalidate cache directory entries. Anthony does not cure the deficiencies of Ishimi and Baron discussed above with reference to claims 1 and 8, upon which claims 7 and 14 depend. Thus, claims 7 and 14 are patentable over Ishimi in view of Baron and Anthony for at least the reasons advanced with reference to claim 1.

Claims 6 and 13 were rejected under 35 U.S.C. § 103 as being unpatentable over Ishimi and Baron and Official Notice. The Examiner relied on Official Notice to cite different cache replacement algorithms. The particular cache replacement algorithm does not cure the deficiencies of Ishimi and Baron discussed above with reference to claims 1 and 8,

upon which claims 6 and 13 depend. Thus, claims 6 and 13 are patentable over Ishimi and Baron for at least the reasons advanced with reference to claim 1.

In view of the foregoing remarks and amendments, Applicants submit that the above-identified application is now in condition for allowance. Early notification to this effect is respectfully requested.

If there are any charges with respect to this response or otherwise, please charge them to Deposit Account 09-0463.

Respectfully submitted,

By:_____

David A. Fox
Registration No. 38,807
CANTOR COLBURN LLP
55 Griffin Road South
Bloomfield, CT 06002
Telephone (860) 286-2929
Facsimile (860) 286-0115
Customer No. 46429

Date: September 7, 2006